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Centro Nacional de Supercomputación

European HPC RISC-V Roadmap Workshop @ HiPEAC 2023

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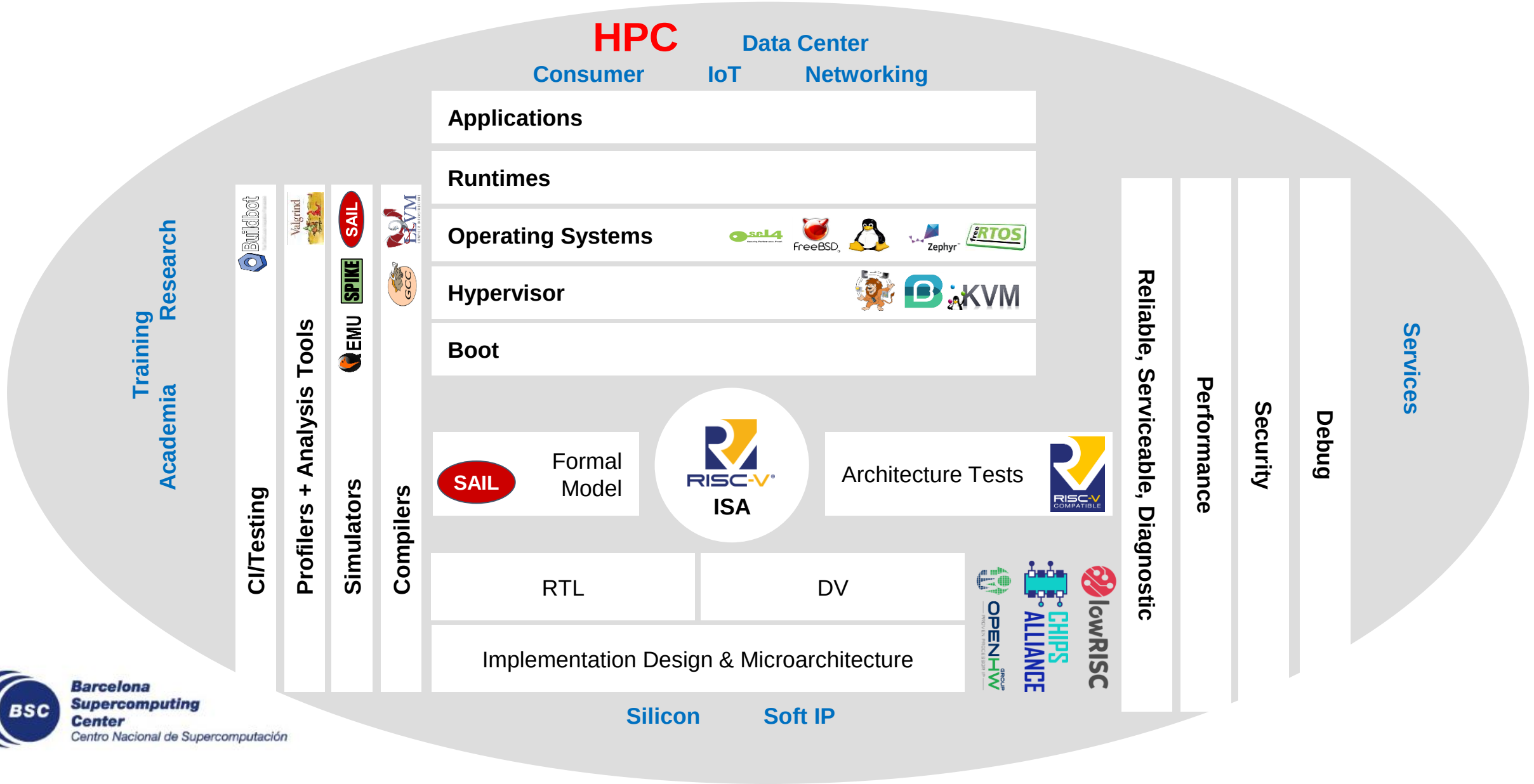
Overview

- RISC-V Ecosystem
- SIG HPC
- RISC-V Research
- RISC-V is HPC!

RISC-V Ecosystem



Special Interest Group for HPC

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SIG-HPC Vision & Mission: RISC-V: IoT to *HPC*

Vision:
The technical and strategic imperatives that guide the RISC-V ecosystem development to enable an Open HPC Ecosystem…

Mission:
…enable RISC-V in a broader set of new software and hardware opportunities in the High Performance Computing space, from the edge to supercomputers, and the software ecosystem required to run legacy and emerging (AI/ML/DL) HPC workloads.

SIG-HPC: An Open era of HPC!

- CPUs, Accelerators, other hardware units, and coprocessors
- Verification and compliance infrastructure and methodologies specific to HPC
- Alignment and engagement and IP enablement.
- RISC-V software ecosystem alignment
- Engage and represent RISC-V in compute intensive industry and academic events
- Identify key industrial and academic partners.
- Support global technology independence with a RISC-V ecosystem roadmap and partners

SIG-HPC Initiatives

- Guide and enable the community
  - Virtual Memory
    - SV57, SV57K, SV64, SV128
  - HPC SW & HW ecosystem & roadmap
  - Accelerators
  - ISA Extensions
  - HPC Software Stack
    - Starting with HPC Libraries
  - RISC-V Testbeds
  - Adapters/Devices: Infiniband, GPUs, etc.

Join the RISC-V Int'l SIG HPC

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RISC-V HPC Research in Europe

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European RISC-V R&D

- 2019: What is Open Source Hardware??
- 2020: Open Source Hardware
- 2021: RISC-V? Roadmap?
  - November roadmap report
  - Horizon Europe Work Programme 2021-22:
    - Open Source Hardware (OSH) appears 6 times
    - CSA Roadmap
- 2022: Build RISC-V!!!
  - KDT JU Work Programme 2021 v13:
    - RISC-V appears 25 times / OSH appears 2 times
  - EU Chip Act (collection of documents)
    - RISC-V and OSH appears 5 each
- 2023 has more to come! (EuroHPC, KDT/Chip JU, etc.)
  - TRISTAN, ISOLDE, …

European Processor Initiative

MEEP
MareNostrum Experimental Exascale Platform

eProcessor

THE EUPILOT

TRISTAN

ISOLDE

⋮

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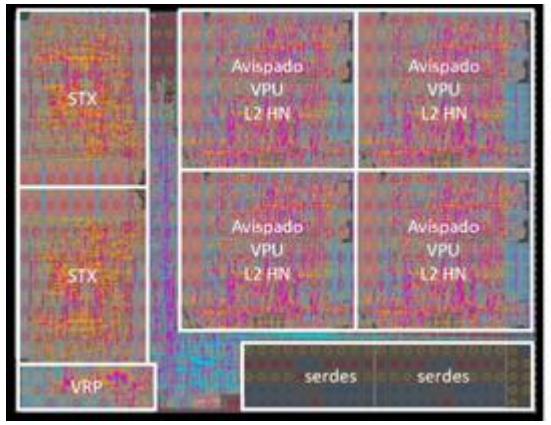
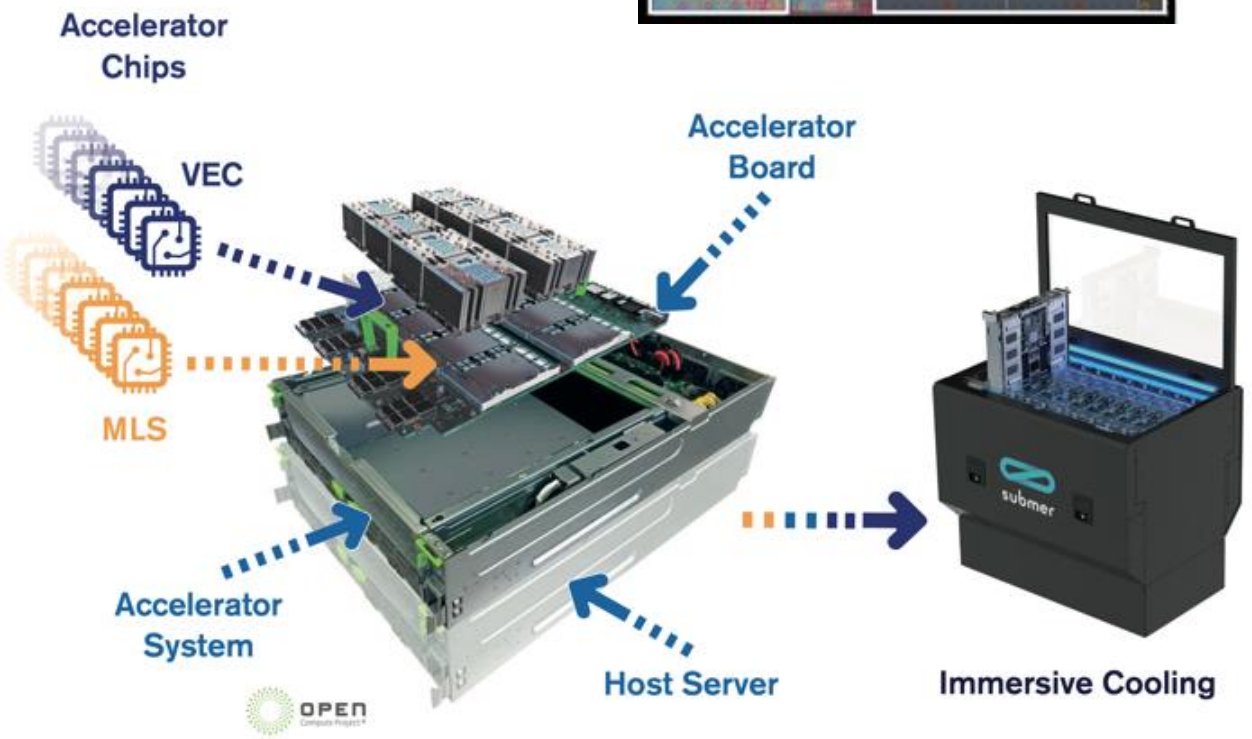
RISC-V Hardware Activities

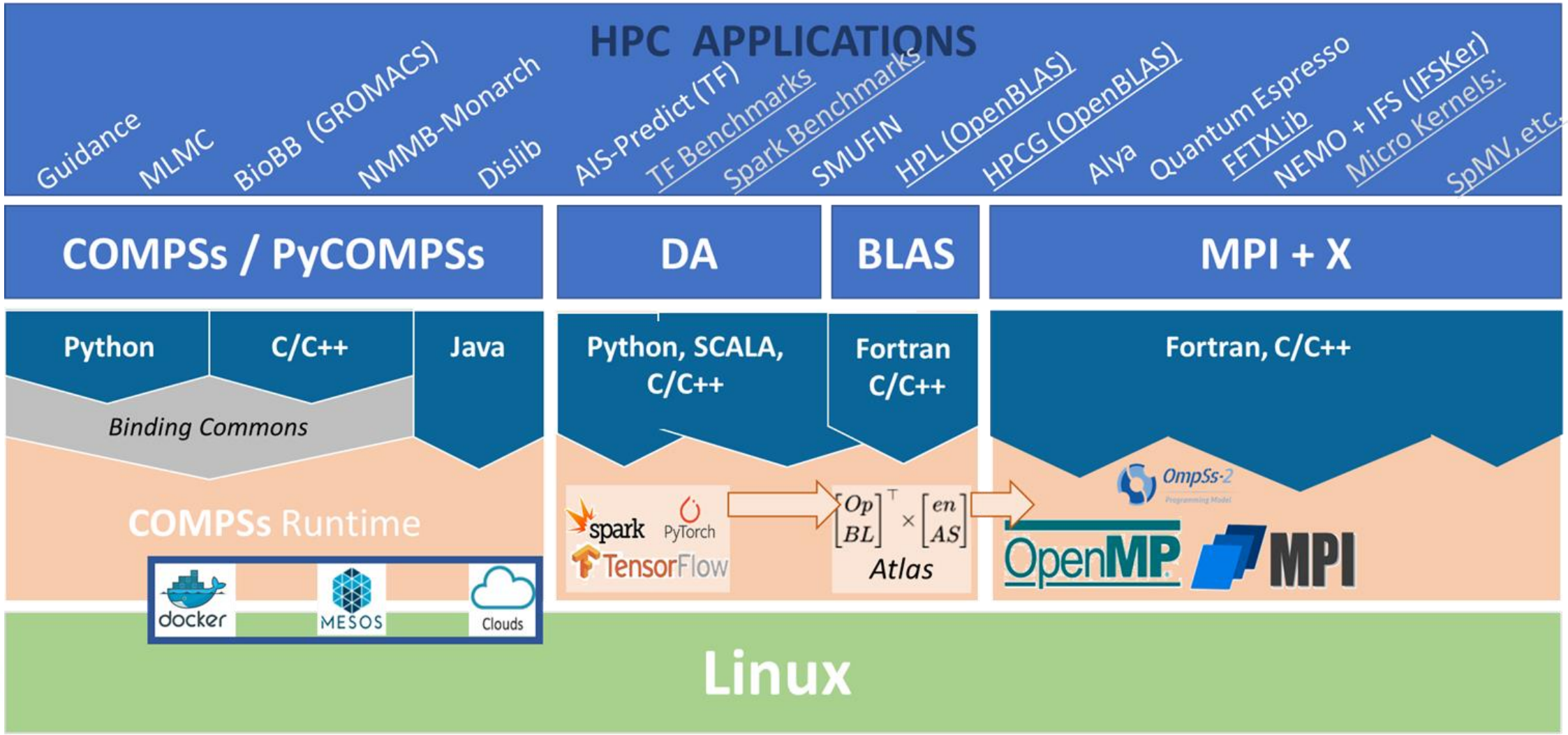
- EPI
  - Vector Processor
  - Machine Learning and Stencil accelerator
  - Variable Precision CPU (High Precision)
- MEEP
  - Vector and systolic arrays coprocessors
- eProcessor
  - OOO Single and multicore chips
- EUPILOT
  - Pilot RISC-V Accelerator Systems
- Many others not mentioned here…



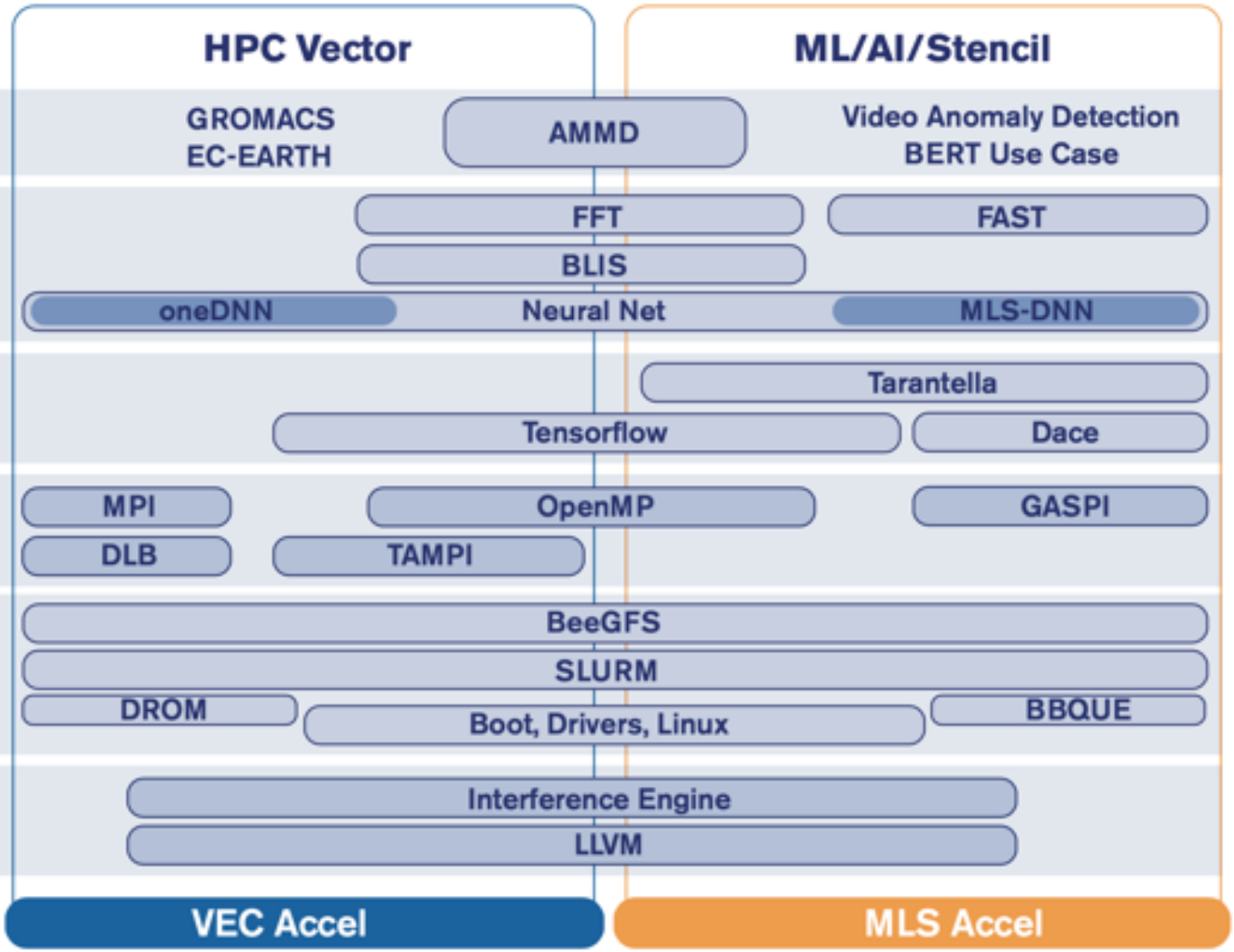


RISC-V Software Activities

MEEP
MareNostrum Experimental Exascale Platform



RISC-V Software Activities



THE EUPILOT

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RISC-V is HPC!

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RISC-V Fan Favorite @ ISC'22 HPC Cluster Competition

- HPC Student Cluster Competition
- Bring your own cluster, < 3KW
- Benchmarking
  - HPCG, HPL, HPCC
- 3 Applications
  - Compile and Run
  - NWChem, ICON, Xcomact3d
- Secret application @ ISC: Fall3D
- Cluster from BSC (7) and Uni. Bologna (6)
  - 300 W cluster
  - 1 GbE
- https://youtu.be/76VOM59bJkY

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HPC RISC-V Companies

Superscalar Out-of-Order Vector-capable Application cores:

- Akeana
- Alibaba
- Andes
- Axelera
- Esperanto (1000 vector core chip)
- InspireSemi (2560 core chip)
- Rivos
- Semidynamics
- SiFive
- TensTorrent (Ascalon core)
- Ventana (chiplets)
- + more (apologies for any missing names)

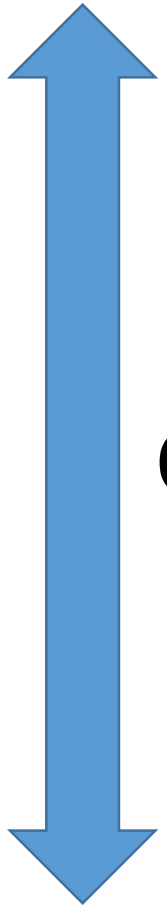
Next HPC RISC-V Project

- EuroHPC JU project announcement, Call published Dec 16th…
  - https://eurohpc-ju.europa.eu/framework-partnership-agreement-fpa-developing-large-scale-european-initiative-high-performance_en
    - Publication date: 15 December 2022
    - Opening date: 26 January 2023
    - Deadline date: 04 April 2023, 17:00 (CEST)
  - 6 years, Multiple SGAs
- Framework Partnership Agreement to:
  1. RISC-V hardware: addressing the design, [d]evel[o]pment, testi[n]g tape-out of different generations of energy efficient high-end processors and/or accelerators, [e.g.] partitioning chiplet [b]ased approaches, for High Performance Computing (HPC), …
  2. integration in test-beds and at least [o]ne pilot [in] pre-operational environments …
  3. RISC-V software: develop the full SW stack and the associated software ecosystem for the developed processors and/or accelerators….
  4. Develop and/or adapt the other necessary technologies for the integration of the RISC-V based components into industrial grade HPC solutions.
  5. Identify the most critical HPC applications and domains and work towards porting and optimising them for the new RISC-V based environment…
  6. Explore and exploit existing manufacturing capabilities in Europe…

270 M€

Join us @ BSC

- Come help us build the Open HPC Ecosystem
- Engineers to Post Docs in:
  - Applications
  - Performance profiling & Tools
  - System Software
  - MPI & OpenMP
  - LLVM Compiler
  - Low-level software
  - Computer Architecture
  - RTL Design
  - Design Verification
  - FPGA Design & Implementation
  - CAD tools
  - HW & SW CI/CD
  - Physical Design



OPEN

AYLA, AI, Containers, etc. — Applications

OpenMP — Libraries/Platforms

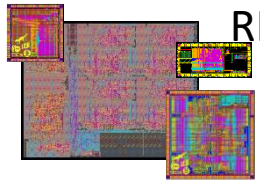
COMPS — Schedulers

LLVM — Compiler/Toolchain

Linux — OS

OCP — HW Systems

RISC-V — CPUs/GPUs/ASICs



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Thank you

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